

**PRESENTATION OF AMARGO:
AN HIERARCHICAL VLSI
PHYSICAL LAYOUT SYNTHESIS SYSTEM**

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ABSTRACT

This work describes AMARGO, an hierarquical environment for general cell VLSI routing, which consists of a number of procedures as a global router, a router for power and ground lines and a channel rounter AMARGO belongs to the Cp2 project: Parallel Processing Contributions: Advances in Microelectronics and in Computer Architecture under development at the Instituto de Informática of the Federal University of Rio Grande do Sul - Brazil

KEY-WORDS:

general cell - VLSI routing - channel routing - Cp2

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I. INTRODUCTION

This paper will describes AMARGO (in portuguese, AMBiente para Automação do Roteamento Geral de CircuiOs), an interactive placement and a automatic routing tools. These tools belong to the layout synthesis abstraction level. The modularisation's strategy of this tool, the proposed algorithms and the obtained results in each software module will be briefly presented.

AMARGO can be classified as a "general-cell" layout synthesis system to be used in the final assembly of the circuit into the chip. The utilisation of this tool is fundamental in the physical layout phase of complex integrated circuits.

Some complex I.C. developed at the Microelectronics Group (GME) of the Federal University of Rio Grande do Sul as RISC microprocessor (PCIR) and a graphics controller (CVTX), had the layout synthesis phase restricted to the mask definition of some main blocks without completing the interconnections between them due to the absence of appropriate tools.

Layout systems that address the same problem as AMARGO have been manufactured by great software vendors, at costs higher than US\$ 50.000. In spite of this extreme extensive cost, many drawbacks can be imputable to these commercial tools. This increases the complexity in the development of a layout physical synthesis system as AMARGO.

II DESCRIPTION OF THE AMARGO SYSTEM

To use the AMARGO system the I.C. designer must provide the synthesis of the functional blocks of the circuit. These blocks can be obtained automatically, by the activation of module generators and choice of the blocks parameters, or since the retrieval of appropriate cells from a cell's library.

Once the layout of all modules of a specif circuit under design is completed, the interconnections among them must be established. This interconnections definition may be done interactively, by the appointment of the connectors which belong to

each interconnection (net) or by a description of a text-file as the described below in table 1.

```
$ NET  
< name-net >  
< name-conector> <instance which the connector belongs to >  
. . .  
< name-conector> <instance which the connector belongs to >
```

Table 1: Text-file of a Net

In fig. 1 it is showed a possible configuration to the system's input. In this case four functional blocks must be interconnected.

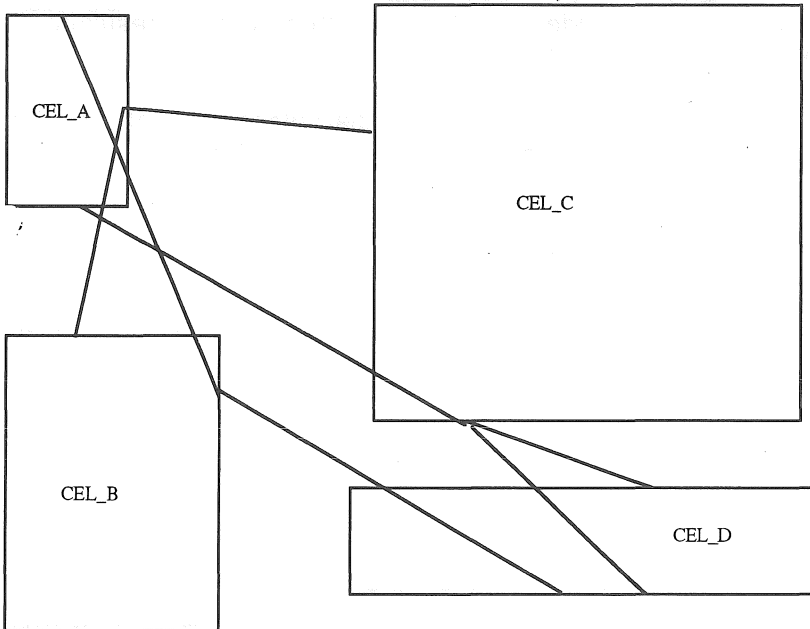


Fig. 1 - Possible configuration to AMARGO's input

Once completed the relative placement (the position of the blocks is not fixed) added to the definition of the nets of the circuit, the AMARGO system's activation will proceed the following tasks:

- 1) initial placement adjustment;
- 2) global routing;
- 3) power lines routing;
- 4) channels ordering;
- 5) channel routing.

All these tasks are performed automatically. Meanwhile the designer can influence by the bias of the algorithms parametrization. To facilitate the results interpretation task, reports containing many relevant statistics are generated in each phase. These reports can be re-used by systems which allow decisions re-evaluation providing then backtracking.

To allow the global routing, it must be obtained a placement graph. The connectors of the blocks that will be interconnected are added to the placement graph, resulting in the so-called complete graph.

If it is disponible the initial placement of fig. 2-a, its corresponding global routing is showed in fig. 2-b.

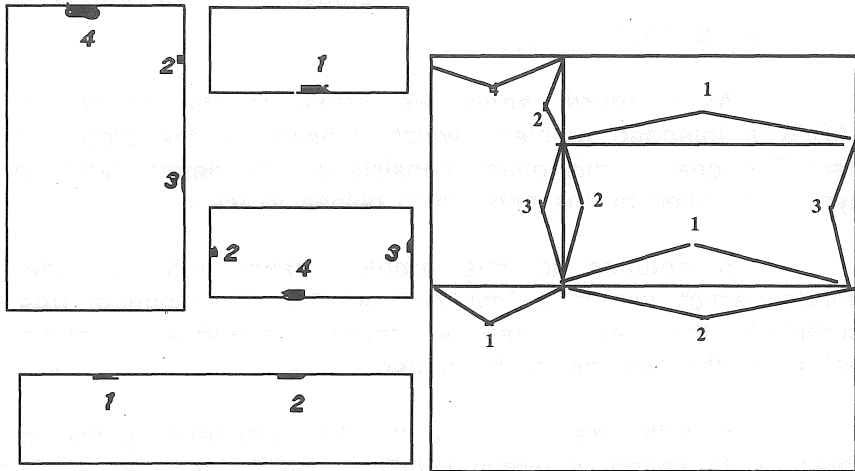


Fig. 2 - Example showing an initial placement and the corresponding complete graph.

The AMARGO system solves the generical routing problem taking into consideration a divide-to-conquer methodology. This is done to keep in reasonably levels the complextiy of the envolved task.

Initially, all routing areas are identified. This is accomplished to obtain all free spaces to the routing task. The solution to this problem employs the corner-stitching data structure technique. In this sense all rectangles are mapped, even the empty spaces.

Secondly, the transparecny over-the-cell channels are established to determine which net will take each transparency of the modules. This claims to minimize the routing area. A solution to this problem consists on the determination of the minimum bounding box (MBB) which contains all net's connectors. To each transparency T of a block B; the following tasks must be performed:

- prepare a list of nets which MBB includes the block into consideration;
- choice of a net, taking into consideration factors as priority and net of the largest channel's length (trying to avoid it)

As a third step, an adjustment of the placement is performed. This allows to verify if there is sufficient space between the blocks to constitute routing areas. A solution to this

problem evolves the utilisation of statistics. More details about this task can be found in [1].

As a fourth step we arrive to the Kernel of the AMARGO's intended problem, which consists of the global routing phase. The goal in this phase consists on the determination of the "ways" to be used by the nets which belong to the circuit.

A solution to this problem takes into consideration methods which search a "minimum way" or a "minimum tree". To accomplish this, each net is treated individually, introducing penalties to that last net to be routed.

A better way to solve the NP complexity global routing problem is to search a global solution considering not a "minimum tree". but a "minimum forest".

In the minimum forest approach, a global solution is optimized presenting the following characteristics:

- independence of the nets ordering
- simultaneity of the development of all trees.

The minimum forest solution employs extensively graphs to model the routing problem, not only preparing placement graphs as connectors graphs .

As the corner-stitching is employed the topological and geometrical models are joined together. In the solution, each vertex corresponds to an intersection between rectangles and each edge corresponds to a congested space.

The proposed and original minimum forest algorithm is presented in table 2.

- A) Starting from an empty graph;
- B) the minimum weight edge to be introduced in the graph is chosen. This edge cannot produce cycles with the other net's edges;
- C) The B step is repeated until all connectors of the nets be connected.

Table 2 - Proposed Minimum Forest Algorithm

As a fifth step the power lines routing (GND/VDD) is produced aiming to minimize the potential drops and metallic migration in the routing and dimensioning of the VDD and GND tracks task. To accomplish this, the power lines global routing is performed prior to the other nets. The determination of each line's width depends on statics and dynamics factors. Finally, a detailed routing is performed

As a sixty step the ordering of the channels is accomplished. This step has as goal the establishment of a chronological order for the channels routing avoiding interferences among them.

As a seventh step the complex channel routing phase is performed. In the case of the AMARGO system, a channel router tool yet developed at GME, named SCHAROP was employed. For more details the [2] reference is suggested.

III. CONCLUSIONS

The present situation of the AMARGO project is the following:

- Graphics interface: implemented and tested.
- Data structure interface: specified and 80% implemented. This interface was developed having in mind a future data base management system integration.
- All main AMARGO's routing steps had their algorithms entirely specified and many of the them completely implemented.

The hardware and software platform used in the project consists of a IBM - PC microcomputer.

As the system under design is extremely complex, the implemented platform is far from being the ideal. As a sequence of this project, it is intended to employ more sophisticated environments, as SUN/UNIX workstations.

REFERENCES

[1] PEREIRA, C. E. ; BARONE, D. A. C. SCHAROP - A Detailed Channel Router. In: IV Brazilian Microelectronics Society Congress, Porto Alegre, july 12-14, 1989. Proceedings. p. 849-859

[2] PEREIRA, C. E.. AMARGO: An hieranchal environment for integrated circuits assembly. M. Sc. dissertation. Pós-Graduação em Ciência da Computação, Porto Alegre, 1990.